IN THE CLAIMS

Please amend the claims as follows:

Claims 1-4 (Canceled).

Claim 5 (Currently Amended): A semiconductor memory device comprising:

a silicon substrate of a first conductivity type having a grid trench extending in two mutually orthogonal directions in an upper major surface thereof, the trench having a trench width A;

a plurality of silicon columns formed on the major surface of the substrate and having a square upper surface defined by the trench, the square upper surface having a side length;

a plurality of transistors each formed on a side surface of the respective silicon columns, each of the transistors comprising:

a first impurity layer formed on the square upper surface of corresponding one of the silicon columns and serving as one of a source and a drain;

a second impurity layer formed on a bottom of the trench adjacent to the corresponding one of the silicon columns and serving as the other of the source and the drain;

a channel portion formed on a side surface of the corresponding one of the silicon columns between the first impurity layer and the second impurity layer;

a gate insulating film formed on the channel portion; and

a gate electrode formed over the channel portion; the gate electrode being formed over the channel portion with the gate insulating film interposed therebetween;

a plurality of capacitors each having two electrodes, one of the two electrodes being connected to the first impurity layer;

a connection line configured to bring the second impurity layer, which is connected to the second impurity layer of an adjacent one of the transistors, out to the major surface of the silicon substrate; and

a bit line formed above the major surface of the silicon substrate,

wherein the connection line is insulatively buried in the trench so as to extend from the second impurity layer on the bottom of the trench to an upper side of the trench and be connected to the bit line, and

wherein the plurality of silicon columns form an array of a matrix form and one pair of the silicon columns at both corners on a diagonal line of the matrix form are lacking.

Claim 6 (Previously Presented): The semiconductor memory device according to claim 5, wherein the width of the trench is equal to the side length of the upper surface of the respective silicon columns.

Claim 7 (Original): The semiconductor memory cell according to claim 5, wherein the plurality of capacitors are formed on the plurality of silicon columns, respectively, each of the capacitors comprising

a capacitor electrode connected to the first impurity layer and being the one electrode;

a dielectric film formed on the capacitor electrode; and

a storage electrode opposing the capacitor electrode through the dielectric film.

Claim 8 (Previously Presented): The semiconductor memory device according to claim 7, wherein each of the capacitors has a planar size that is substantially the same as a size of the upper surface of the silicon column.

Claims 9-10 (Canceled).

Claim 11 (Previously Presented): The semiconductor memory device according to claim 5, wherein the gate electrode is so formed as to surround the corresponding one of the silicon columns and, wherein the gate electrodes of the silicon columns aligned in one direction are connected to form a word line and the connection line is formed in the trench at a central area surrounded by mutually adjacent four of the silicon columns.

Claim 12 (Previously Presented): The semiconductor memory device according to claim 5, wherein the gate electrode is formed on one side surface of the corresponding one of the silicon columns and, wherein the gate electrodes of the silicon columns aligned in one direction are connected to form a word line and the connection line is formed in the trench along another side surface adjacent to the one side surface of the corresponding one of the silicon columns.

Claim 13 (Previously Presented): The semiconductor memory device according to claim 5, wherein an aligning pitch of the silicon columns in an extending direction of the bit line is made loose at a site where the second impurity layer is connected to the connection line at the bottom of the trench.

Claim 14 (Previously Presented): The semiconductor memory device according to claim 5, wherein the second impurity layer is formed as a band configuration around a corresponding one of the silicon columns.

Claim 15 (Original): The semiconductor memory device according to claim 5, wherein the second impurity layer is united with respect to adjacent three or more of the silicon columns on the bottom of the trench.

Claims 16-21 (Canceled).

Claims 22 (Currently Amended): A semiconductor memory device comprising:

a silicon substrate of a first conductivity type having a grid of trench extending in two mutually orthogonal directions in an upper major surface of the silicon substrate, the trench having a trench width;

a plurality of silicon columns formed on the major surface of the substrate and having a square upper surface defined by the trench, the square upper surface having a side length;

a plurality of [[the]] transistors each formed on a side surface of the respective silicon columns, each of the transistors comprising

a first impurity layer formed on the square upper surface of corresponding one of the silicon columns and serving as one of a source and a drain;

a second impurity layer formed on a bottom of the trench adjacent to the corresponding one of the silicon columns and serving as the other of the source and the drain;

a channel portion formed on a side surface of the corresponding one of the silicon columns between the first impurity layer and the second impurity layer;

a gate insulating film formed on the channel portion; and

a gate electrode formed over the channel portion with the gate insulating film interposed therebetween;

a plurality of capacitors each having two electrodes ~~electrode~~, one of the two electrodes being connected to the first impurity layer;

a connection line configured to bring the second impurity layer, which is connected to the second impurity layer of an adjacent one of the transistors, out to the major surface of the silicon substrate; and

a bit line formed above the major surface of the silicon substrate,

wherein the connection line is insulatively buried in the trench so as to extend from the second impurity layer on the bottom of the trench to an upper side of the trench and be connected to the bit line, and

an aligning pitch of the silicon columns in an extending direction of the bit line is made loose at a site where the second impurity layer is connected to the connection line at the bottom of the trench.

Claim 23 (Currently Amended): A semiconductor memory device comprising:

a silicon substrate of a first conductivity type having a grid of trench extending in two mutually orthogonal directions in an upper major surface of the silicon substrate, the trench having a trench width;

a plurality of silicon columns formed on the major surface of the substrate and having a square upper surface defined by the trench, the square upper surface having a side length;

a plurality of the transistors each formed on a side surface of the respective silicon columns, each of the transistors comprising

a first impurity layer formed on the

square upper surface of corresponding one of the silicon columns and serving as one of a source and a drain;

a second impurity layer formed on a bottom of the trench adjacent to the corresponding one of the silicon columns and serving as the other of the source and the drain;

a channel portion formed on a side surface of the corresponding one of the silicon columns between the first impurity layer and the second impurity layer;

a gate insulating film formed on the channel portion; and

a gate electrode formed over the channel portion with the fate insulating film interposed therebetween;

a plurality of capacitors each having two electrodes ~~electrode~~, one of the two electrodes being connected to the first plurality layer;

a connection line configured to bring the second impurity layer, which is connected to the second impurity layer of an adjacent one of the transistors, out to the major surface of the silicon substrate; and

a bit line formed above the major surface of the silicon substrate,

wherein the connection line is insulatively ~~insulative~~ buried in the trench so as to extend from the second impurity layer on the bottom of the trench to an upper side of the trench and be connected to the bit line, and

the second impurity layer is united with respect to adjacent three or more of the silicon columns on the bottom of the trench.